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12/23/2004

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EXAMINER

WOOD, WILLIAM H

ART UNIT

PAPER NUMBER

2124

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/637,078

Applicant(s)

ALTMAN ET AL.

Examiner

William H. Wood

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-16,18-30 and 32-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-16,18-30 and 32-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

Claims 1, 3-16, 18-30 and 32-42 are pending and have been examined.

#### ***Drawings***

1. The drawings were received on 09 August 2004. These drawings will not be entered as the constitute new matter.

#### ***Specification***

2. The drawing amendment filed 09 August 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: newly amended figure 1 does not correlate to originally filed claim 1; originally two arrows extended into element 102, amendment now shows one arrow extending away from element 102. Applicant is required to cancel the new matter in the reply to this Office Action.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 1, 4-8, 11-13, 16-17, 22, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy** et al. (USPN 6,622,300).

Claim 1

**Krishnaswamy**'s background disclosed a method for profiling computer program executions in a computer processing system having a processor and a memory hierarchy (*column 1, lines 10-43*), comprising the steps of:

- ♦ executing a computer program (*column 1, lines 33-35*);
- ♦ storing, in a memory array, profile counts for a plurality of events associated with the execution of the computer program (*column 1, lines 36-39*)
- ♦ updating the profile counts for only the events (*column 1, lines 33-37*); and
- ♦ assisting compilation and optimization of the computer program, based upon the profile counts stored in the memory array (*column 1, lines 33-43*).

**Krishnaswamy**'s background did not explicitly state selected events or separate memories. However, **Krishnaswamy** later demonstrated that it was known at the time of invention to select events for profiling (*column 6, lines 21-30*) and separate memories (*column 6, lines 28-29*). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling-based optimizing compiler of **Krishnaswamy** with selecting events as found in **Krishnaswamy**'s own teaching, and furthermore it would have been obvious to implement the optimizing compiler of **Krishnaswamy** with a separate memory for monitoring performance/profiling as suggested by **Krishnaswamy**'s teaching. This implementation would have been obvious

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because one of ordinary skill in the art would be motivated to utilize a preferred method of profiling (column 6, line 21) that reduces code interference and provides the varying functionality provided by performance monitoring units, such as that described above.

Claim 4

**Krishnaswamy** disclosed the method according to claim 1, wherein said updating step is triggered by execution of the events (*column 6, lines 21-33*).

Claim 5

**Krishnaswamy** did not explicitly state the method according to claim 1, wherein said updating step is triggered by execution of instructions embedded into an instruction stream of the computer program. **Krishnaswamy** demonstrated that it was known at the time of invention to instrument code for profiling (*column 1, lines 56-57*). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling-based optimizing compiler of **Krishnaswamy** with instrumented code as found in **Krishnaswamy's** own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to allow for collection of a minimum amount of data, thus saving space and time (*column 1, lines 60-62*), additionally not all processors are equipped with performance monitoring functions and thus instrumentation is required for profiling.

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Claim 6

**Krishnaswamy** disclosed the method according to claim 1, further comprising the step of detecting whether a profile count has exceeded an adjustable predefined threshold (*column 6, lines 30-34*).

Claim 7

**Krishnaswamy** disclosed the method according to claim 1, further comprising the step of indicating when a profile count has exceeded an adjustable predefined threshold (*column 6, lines 30-34*).

Claim 8

**Krishnaswamy** disclosed the method according to claim 7, wherein said indicating step comprises the step of raising an exception (*column 6, lines 30-34*).

Claim 11

**Krishnaswamy** disclosed the method according to claim 1, further comprising the step of identifying profile information corresponding to the profile counts using a profiling event identifier (*column 6, lines 26-36; column 1, lines 34-43; identification of some sort required for proper usage of collected information*).

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Claim 12

**Krishnaswamy** disclosed the method according to claim 11, further comprising the step of addressing the memory array, using the profiling event identifier (*column 6, lines 24-36; column 1, lines 34-43; identification of some sort required for proper usage of collected information*).

Claim 13

**Krishnaswamy** disclosed the method according to claim 1, further comprising the steps of: generating the profile counts using profile counters associated with the events (*column 6, lines 24-28*). **Krishnaswamy** did not explicitly state maintaining the profile counters in a set-associate manner. Official Notice is taken that it was known at the time of invention to store values in a set-associative manner. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the memory of **Krishnaswamy** with a set associative manner. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of a regular method of memory, which thus common and easy to use/implement.

Claim 16

**Krishnaswamy** disclosed the method according to claim 1, further comprising the step of supporting read operations from the memory array in an off-line optimization of the program (*column 1, lines 30-43*).

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Claim 17

**Krishnaswamy** disclosed the method according to claim 1, further comprising the step of assisting optimization of the program, based upon the profile counts stored in the memory array (*column 1, lines 34-37*).

Claim 22

**Krishnaswamy** disclosed the method according to claim 1, wherein the memory hierarchy includes data and instruction caches, and the memory array is separate and distinct from the memory hierarchy so as to not perturb normal operations of the data and instruction caches (*Figure 2; and as above for claim 1*).

Claim 38

**Krishnaswamy** disclosed the method according to claim 1, wherein said method is implemented by a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform said method steps (*column 1, lines 34-37; compiler*).

5. Claims 3, 9-10, 23-30, 32-34, 37 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy et al.** (USPN 6,622,300) in view of "Dictionary of **Computing**".



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Claim 3

**Krishnaswamy** did not explicitly state the method according to claim 1, wherein said storing and updating steps are performed asynchronously to prevent a decrease of an execution speed of the computer program. **Computing** demonstrated that it was known at the time of invention to perform circuit operations asynchronously (page 26, asynchronous circuit). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the system of **Krishnaswamy** with an asynchronous circuit design, including storing and updating counts as suggested by **Computing's** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to allow operation with a minimum of delay (page 26, asynchronous circuit).

Claim 9

**Krishnaswamy** disclosed the method according to claim 1, further comprising the steps of: accumulating profile updates (**Krishnaswamy**: column 1, lines 34-37).

**Krishnaswamy** did not explicitly state dividing the accumulated profile updates by a threshold fraction. **Computing** demonstrated that it was known at the time of invention to make use of scaling (page 432). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling counters of **Krishnaswamy** with scaling (or dividing/multiplying by a threshold fraction) the update value as found in **Computing's** teaching. This implementation would have been obvious because one of

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ordinary skill in the art would be motivated to adjust the stored value to the hardware/equipment (register size) limitations (**Computing**: page 432).

Claim 10

**Krishnaswamy** did not explicitly state disclosed the method according to claim 1, further comprising the step of scaling the profile counts to prevent profile information overflow. **Computing** demonstrated that it was known at the time of invention to make use of scaling (page 432). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling counters of **Krishnaswamy** with scaling the update value as found in **Computing**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to adjust the stored value to the hardware/equipment (register size) limitations (**Computing**: page 432).

Claim 23

The limitations of claim 23 correspond to the limitations of claims 1 and 10 and as such are rejected in the same manner.

Claims 24-30, 32-34, 37 and 39

The limitations of claims 24-30, 32-34, 37 and 39 correspond to the limitations of claims 3-9, 11-13, 22 and 17 and are dependent upon claim 23. Thus, the claims are rejected in the same manner as 3-9, 11-13, 22 and 17 in consideration of claim 23.

6. Claims 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy** et al. (USPN 6,622,300) in view of **Record** et al. (USPN 5,355,484).

Claims 14 and 15

**Krishnaswamy** did not explicitly state the method according to claim 13, further comprising the step of selecting a profile counter to be evicted from the memory array based upon a predefined replacement, when a number of profiling events assigned to an associative class of events is exceeded. **Record** demonstrated that it was known at the time of invention to perform the above operation (column 9, lines 13-20). **Record** further demonstrated (as found in claim 15) that it was known at the time of invention to utilize the replacement strategy based upon on of least-recently-used and first-in-first-out (column 9, lines 13-20). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the optimizing profiling system of **Krishnaswamy** with the control provided by **Record**. This implementation would have been obvious because one of ordinary skill in the art would be motivated to minimize any reduction in execution time resulting from profiling a system by limiting the number of events to be monitored (**Record**: column 2, lines 17-25).

7. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy** et al. (USPN 6,622,300) in view of Dictionary of **Computing**" in further view of **Record** et al. (USPN 5,355,484).

Claims 35-36

The limitations of claims 35 and 36 correspond to the limitations of claims 14 and 15 and are indirectly dependent upon claim 23. Thus, the claims are rejected in the same manner as 35 and 36 in consideration of claim 23.

8. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy et al.** (USPN 6,622,300) in view of **Altman et al.**, "DAISY: Dynamic Compilation for 100% Architectural Compatibility".

Claim 18

**Krishnaswamy** did not explicitly state the method according to claim 1, wherein said assisting step is performed during at least one of dynamic binary translation and dynamic optimization [compilation] of the computer program. **Altman** demonstrated that it was known at the time of invention to provide dynamic binary translation and dynamic optimization [compilation] (page 27, section 2 and page 28, section 2.1; additionally page 27, left column, last three paragraphs). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling compiler system of **Krishnaswamy** with dynamic translation and optimization [compilation] as found in **Altman's** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide compiling/translating system with dynamic operation (useful for providing real-time operation; page 27, left

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column, second and third paragraphs) and profiling for optimization (useful for helping code execute better).

Claim 19

**Krishnaswamy** and **Altman** disclosed the method according to claim 18, wherein the dynamic binary translation and dynamic optimization of the computer program results in translated and optimized code, respectively, the translated and optimized code comprising instructions groups which pass control there between (***Krishnaswamy**: column 1, lines 30-43; and **Altman**: page 27, right column, third paragraph; page 29, section 3).*

9. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy** et al. (USPN 6,622,300) in view of **Altman** et al., "DAISY: Dynamic Compilation for 100% Architectural Compatibility" in further view of **Chang** et al., "Using Profile Information to Assist Classic Code Optimizations".

Claims 20 and 21

**Krishnaswamy** and **Altman** did not explicitly state the method according to claim 19, further comprising the step of identifying frequently executed paths of the computer program, by instrumenting exits from the instruction groups with a profiling instruction that indicates a unique group exit identifier. **Chang** demonstrated that it was known at the time of invention to instrument groups of instructions to provide an ID (page 1305-

1306, item (a) under “Profiler implementation”) and to optimize frequently executed paths (page 1306, bottom). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the optimizing profiling compiler of **Krishnaswamy** and **Altman** with group instrumentation as found in **Chang’s** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to optimize frequently executed program paths (page 1301, Introduction). **Chang** did not explicitly state to instrument exit points. Official Notice is taken that it was known at the time of invention to instrument exits. Furthermore, **Chang** demonstrated instrumenting the entry point (page 1305-1306, item (a) under “Profiler implementation”) or taken more generally simply ensuring instrumentation of the group/function. It would have been obvious to one of ordinary skill in the art at the time of invention to instrument exits of groups/functions in the compiler of **Krishnaswamy**, **Altman** and **Chang**. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide an information about the profiled code, which includes determining if a group/function is executed. Both entry and exit points are the most obvious instrumentation points of all locations, since they are easily identifiable. Additionally, **Krishnaswamy** and **Altman** did not explicitly state the method according to claim 19, further comprising the step of extending the instruction groups along a frequently executed path. However, **Chang** demonstrated this as well on page 1306, items (b) through (e) and page 1301-1302, “Introduction”.

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10. Claims 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy** et al. (USPN 6,622,300) in view of **Chang** et al., "Using Profile Information to Assist Classic Code Optimizations".

Claim 40

**Krishnaswamy** disclosed a method for profiling computer program executions in a computer processing system having a processor and a memory hierarchy, comprising the steps of:

- ♦ executing a computer program (*column 1, lines 33-35*);
- ♦ storing, in a single memory array, a plurality of event-specific profile counts, each associated with an event associated with the execution of a path of the computer program (*column 1, lines 36-39*)
- ♦ updating the profile counts for only the events (*column 1, lines 33-37*)

**Krishnaswamy's** background did not explicitly state selected events or separate memories or uniquely assigned counting. However, **Krishnaswamy** later demonstrated that it was known at the time of invention to select events for profiling (column 6, lines 21-30) and separate memories (column 6, lines 28-29) and uniquely assigned counting (column 6, lines 21-28). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling-based optimizing compiler of **Krishnaswamy** with selecting events as found in **Krishnaswamy's** own teaching, and furthermore it would have been obvious to implement the optimizing compiler of **Krishnaswamy** with a separate memory for monitoring performance/profiling as

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suggested by **Krishnaswamy**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize a preferred method of profiling (column 6, line 21) that reduces code interference and provides the varying functionality provided by performance monitoring units, such as that described above.

**Krishnaswamy** did not explicitly state if at least one of the selected event-specific counts has exceeded a predefined threshold, optimizing the portions of the computer program associated with the event-specific profile counts more aggressively than other portions of the computer program. **Chang** demonstrated that it was known at the time of invention to optimize more heavily various parts of a program based upon threshold (pages 1306-1308, "Optimizing frequently executed paths" section). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the optimizing profiling compiler of **Krishnaswamy** with group instrumentation as found in **Chang**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to optimize frequently executed program paths primarily since they are executed more (page 1301, Introduction and pages 1306-1308).

#### Claim 42

**Krishnaswamy** did not explicitly state the method according to claim 40, wherein the memory array is arranged as a two-way set associative array. Official Notice is taken that it was known at the time of invention to store values in a two way set-associative



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manner. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the memory of **Krishnaswamy** with a set associative manner. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of a regular method of memory, which thus common and easy to use/implement.

11. Claims 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Krishnaswamy et al.** (USPN 6,622,300) in view of **Chang et al.**, "Using Profile Information to Assist Classic Code Optimizations" in further view of **Altman et al.**, "DAISY: Dynamic Compilation for 100% Architectural Compatibility".

Claim 41

**Krishnaswamy** did not explicitly state the method according to claim 40, further comprising the step of optimizing the computer program during at least one of static and dynamic compilation using the profile information. **Altman** demonstrated that it was known at the time of invention to provide dynamic binary translation and dynamic optimization [compilation] (page 27, section 2 and page 28, section 2.1; additionally page 27, left column, last three paragraphs). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the profiling compiler system of **Krishnaswamy** with dynamic translation and optimization [compilation] as found in **Altman's** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide compiling/translating

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system with dynamic operation (useful for providing real-time operation; page 27, left column, second and third paragraphs) and profiling for optimization (useful for helping code execute better).

### ***Response to Arguments***

12. Applicant's arguments filed 09 August 2004 have been fully considered but they are not persuasive. Applicant argued: <sup>1)</sup> **Krishnaswamy** does not disclose selecting at least one of a plurality of events for profiling; <sup>2)</sup> **Krishnaswamy** does not provide memory array separate and distinct from the memory hierarchy so as to not perturb normal operations of the memory hierarchy; <sup>3)</sup> no motivation for combination of **Krishnaswamy's** various elements; <sup>4)</sup> no disclosure of a controller as recited in claim 23; <sup>5)</sup> no motivation to combine **Computing** disclosing "scaling"; and <sup>6)</sup> generally no disclosure of claim 40. It is clear from the prior art of record the above issues are disclosed as indicated.

First, **Krishnaswamy** clearly demonstrated a plurality of events (column 1, lines 37-43). Further, **Krishnaswamy** disclosed selecting a plurality of events (column 6, lines 24-28). The counters are *programmable*.

Second, separate memories were disclosed by the **Krishnaswamy** prior art. Note the buffers and caches (column 6, lines 28-29), not to mention the counters themselves. This additional memory has to be accessed from the other "regular" memory (column 6, lines 35-41).

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Third, the explicit motivation for combination is the counter system of **Krishnaswamy** is a “preferred” method of performing profiling optimization (column 6, lines 21-22). Additionally, upon reading the **Krishnaswamy** prior art as a whole, one of ordinary skill in the art would recognize the general concepts of **Krishnaswamy**'s background as obviously being implemented in more specific detail in the rest of **Krishnaswamy**.

Fourth, the controller is inherent to the fact that the PMU element is programmable (column 6, lines 24-28). The PMU hardware must have circuitry for the selection/programming in order to function.

Fifth, motivation was present in the prior art cited (**Computing**: page 432, *scaling*). The definition stated, “adjustment of values to be used in a computation so that they and their resultant values are within the range that can be handled by the process or equipment” (registers in this case).

Sixth, claim 40 has been newly rejected to account for amended limitations.

Thus, having addressed Applicant's raised issues, the rejections are substantially maintained.

### ***Conclusion***

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Correspondence Information***

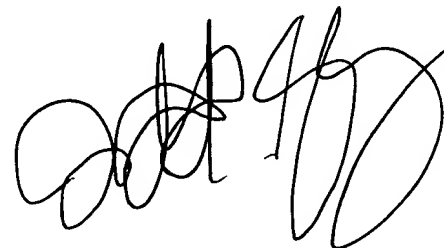
Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)-272-3736. The examiner can normally be reached 9:00am - 5:30pm Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)-272-3719. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.



William H. Wood  
November 30, 2004



**TODD INGBERG  
PRIMARY EXAMINER**